

# Vertical GaN Devices for Power Electronics in Extreme Environments

**Isik C. Kizilyalli<sup>(1)</sup>, Robert J. Kaplar<sup>(2)</sup>, O. Aktas<sup>(1)</sup>, A. M. Armstrong<sup>(2)</sup>, M. P. King<sup>(2)</sup>,  
and J. R. Dickerson<sup>(2)</sup>**

(1) Avogy Inc., 677 River Oaks Parkway, San Jose CA, 95134, USA

(2) Sandia National Laboratories, Albuquerque, NM 87185, USA

There is great interest in wide band-gap semiconductor devices and most recently in monolithic GaN structures for power electronics applications. In this paper vertical p-n diodes and transistors fabricated on pseudo bulk low defect density ( $10^4$  to  $10^6$  cm<sup>-2</sup>) GaN substrates are discussed. Homoepitaxial MOCVD growth of GaN on its native substrate and being able to control doping has allowed the realization of vertical device architectures with drift layer thicknesses of 6 to 40  $\mu$ m and net carrier electron concentrations of  $2 \times 10^{15}$  to  $2.5 \times 10^{16}$  cm<sup>-3</sup>. This parameter range is suitable for applications requiring breakdown voltages of 600V to 5kV and current levels to 400A with a proper edge termination strategy. Vertical GaN devices are studied under cryogenic conditions, radiation, and ruggedness performance under repetitive avalanche stress.

Mg, which is used as a p-type dopant in GaN is a relatively deep acceptor ( $E_A \approx 0.18$ eV) and susceptible to freeze out at temperatures below 200K (Fig. 1). The loss of holes in p-GaN has deleterious effect on p-n junction behavior (Fig. 2), p-GaN contacts, and channel control in junction field-effect transistors at temperatures below 200K. Impact ionization based avalanche breakdown in GaN p-n junctions is characterized between 77K and 423K for the first time. At higher temperatures the p-n junction breakdown voltage improves due to increased phonon scattering (Fig. 3). A positive temperature coefficient in the breakdown voltage is demonstrated down to 77K; however, the device breakdown characteristics are not as abrupt at temperatures below 200K. On the other hand, contact resistance to p-GaN is reduced dramatically above room temperature improving the overall device performance in GaN p-n diodes in all cases except where the n-type drift region resistance dominates the total forward resistance. In this case, the electron mobility can be de-convolved and is found to decrease with  $T^{-3/2}$ , consistent with a phonon scattering model. It is demonstrated that vertical GaN devices (diodes and transistors) utilizing p-n junctions are suitable for most practical applications including automotive ( $210K < T < 423K$ ) but may have limitations for cryogenic operation (77K) due to the freeze-out of Mg (Fig. 4).

Inductive avalanche test results demonstrate that GaN p-n diodes can sustain single-pulse and repetitive inductive avalanche currents. The 0.36 mm<sup>2</sup> vertical GaN p-n diodes can sustain single-pulse avalanche currents as high as 10 A while reverse biased at 1200V. The safe zone of the single pulse avalanche current is limited by peak pulse power and energy deposited in the device. The temperature dependent behavior of the breakdown voltage and the reverse-voltage at onset of avalanche has a positive temperature coefficient. Repetitive avalanche ruggedness testing was performed by applying  $10^5$  pulses at 5 kHz frequency with increasing repetitive stress

current. Based on a population of 63 devices, the incremental failure rate under repetitive avalanche current increases with increasing avalanche current. The devices that survive the step stress test sustain no parametric drift under repetitive avalanche.

The GaN P-N diodes discussed herein have been shown to be robust to irradiation by 2.5 MeV protons and 1 MeV neutrons (Fig. 6). While irradiation up to a fluence of approximately  $3 \times 10^{13}$  cm<sup>-2</sup> does result in an increase in on-resistance and a reduction in breakdown voltage, the unipolar figure-of-merit remains superior to that of un-irradiated Si devices.

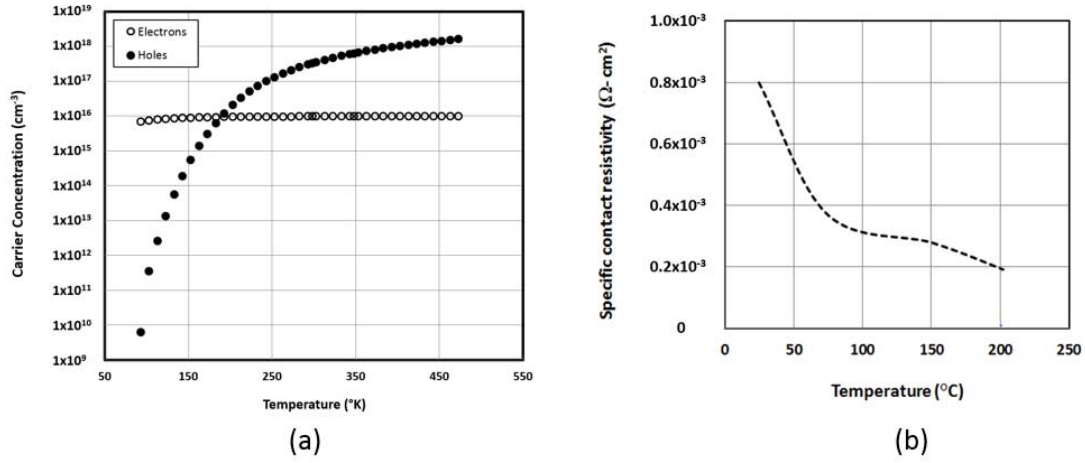
## Acknowledgements

The work at Avogy work was supported in part by U.S. ARPA-E SWITCHES program (Director: Dr. T. Heidel) and the U.S. Office of Naval Research contract N122-135-0058 (Director: Dr. P. Maki). The work at Sandia was supported by the Laboratory Directed Research and Development program. Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

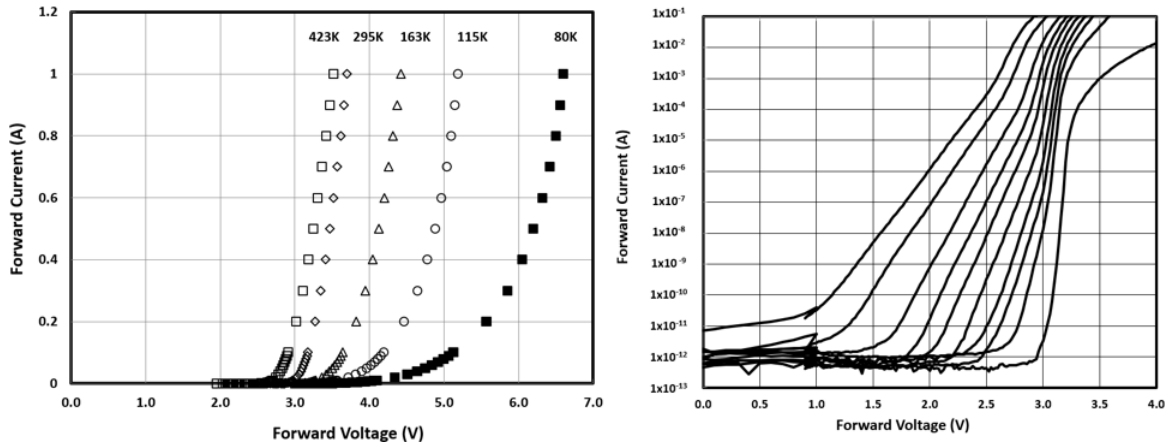
Author Contact Information: [kizilyalli@ieee.org](mailto:kizilyalli@ieee.org).

## References

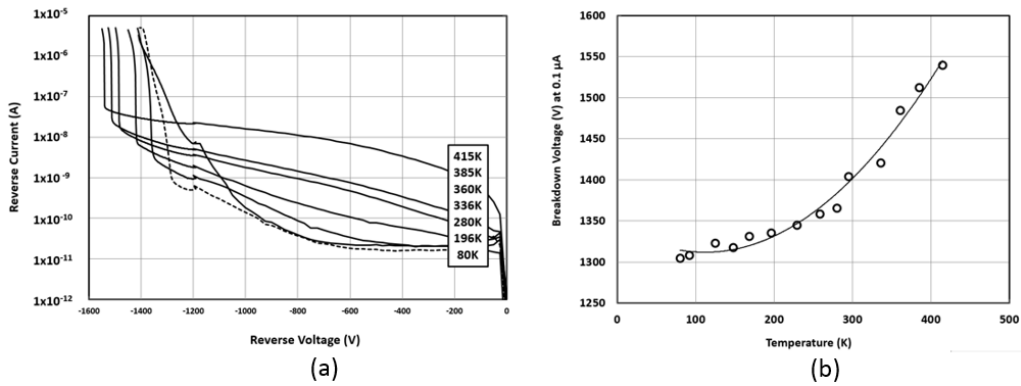
1. I. C. Kizilyalli, P. Bui-Quang, D. Disney\*, H. Bhatia, and Ozgur Aktas, "Reliability Studies of Vertical GaN Devices Based on Bulk GaN Substrates," *Microelectronics Reliability*, vol. 55, pp. 1654-1661, 2015.
2. O. Aktas and I.C. Kizilyalli, "Avalanche Capability of Vertical GaN p-n Junctions on Bulk GaN Substrates," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 890-892, 2015.
3. I. C. Kizilyalli and O. Aktas, "Characterization of vertical GaN p-n diodes and junction field effect transistors on bulk GaN down to cryogenic temperatures," accepted for *Solid State Technologies*, Special Issue on Wide-Band Gap Semiconductors, December, 2015.
4. M.P. King, A. M. Armstrong, G. Vizkelethy, R. M. Fleming, A.A. Allerman, J. Wierer, J. Campbell, W. Wampler, I.C. Kizilyalli, and R.K. Kaplar, "Performance and Breakdown Characteristics of Irradiated Vertical Power GaN P-i-N Diodes," *Proc. NSREC*, 2015.



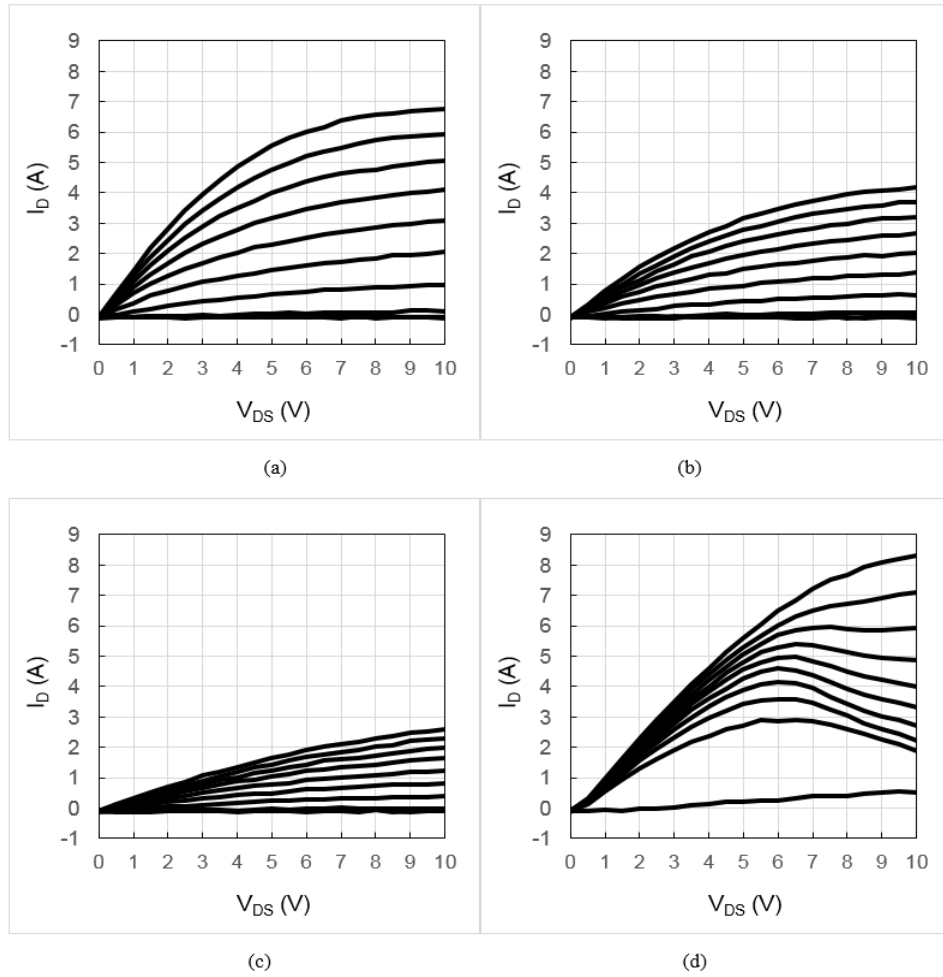
**Figure 1.** (a) Mg freeze-out effect and hole concentration (b) contact resistance versus temperature for p-type GaN.



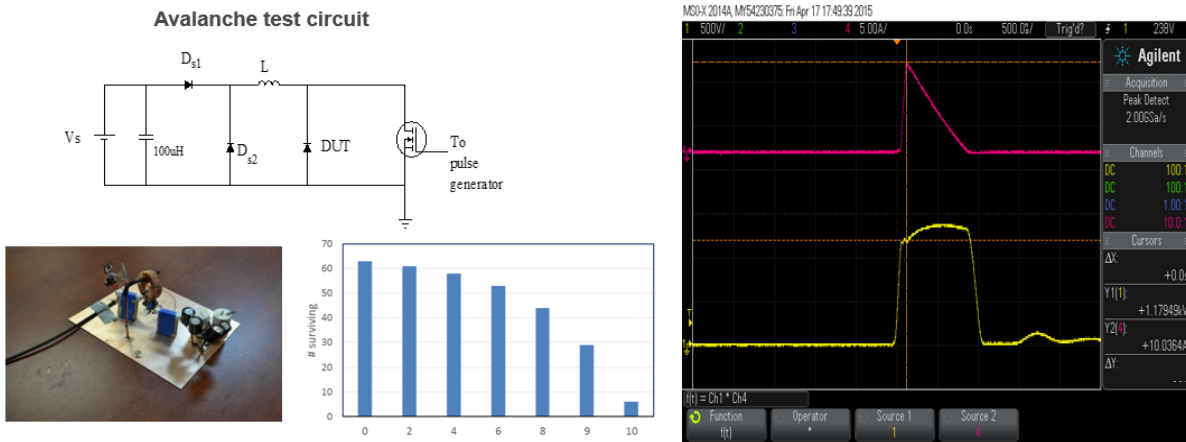
**Figure 2.** Forward I-V characteristics of p-n diodes on a linear (a) and logarithmic scale (b). In (b) 423K, 362K, 295K, 250K, 228K, 196K, 169K, 151K, 129K, and 80K are the measurement temperatures.



**Figure 3.** (a) Reverse I-V characteristics and (b) breakdown voltage of p-n diodes versus the ambient temperature.

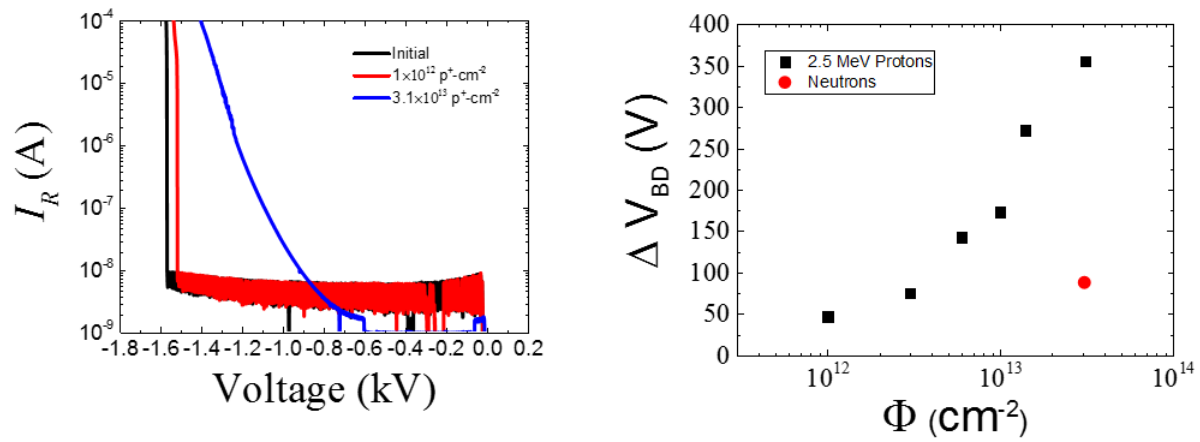


**Figure 4.** Output characteristics of the packaged vertical FETs at a) 123K (-150°C), b) 300K (27°C), c) 423K (150°C), d) 77K (-196°C). The measurements were performed using 300  $\mu$ s voltage pulses. The gate bias was stepped at the following voltage values: -30, -20, -17.5, -15, -12.5, -10, -7.5, -5, -2.5, 0V.



**GaN vertical p-n diodes ( $A=0.36 \text{ mm}^2$ ) can withstand  $10^5$  / 5kHz pulses at 10A and 1200V for 10's of ns**

**Figure 5.** Inductive load avalanche ruggedness of p-n diodes.



**Figure 6.** Vertical p-n diodes under irradiation.